

6-22-04

Ken Zweibel
National Center for Photovoltaics
National Renewable Energy Laboratory, MS 3212
1617 Cole Blvd.
Golden, Co. 80401

Dear Mr. Zweibel:

This is the third quarterly report for the third year (Phase III) of our research under the Thin Film Partnership Program (Subcontract No. ADJ-1-30630-07 to Colorado State University). A brief summary and details of our work are given below. This report is in fulfillment of deliverable D.3.3 of the subcontract statement of work (SOW).

1. Summary

Significant advancements have been made in demonstrating a process for consistently fabricating stable CdTe PV. During the past few months, the optimum, baseline absorber/CdCl₂ process has been repeated for over 9 hours of operation. During these runs the Voc and Jsc of devices with no intentional copper (fabricated up to but not including the back contact processing) have remained consistent. Current efforts are underway to advance the back contact processing to this level of consistency for long duration processing.

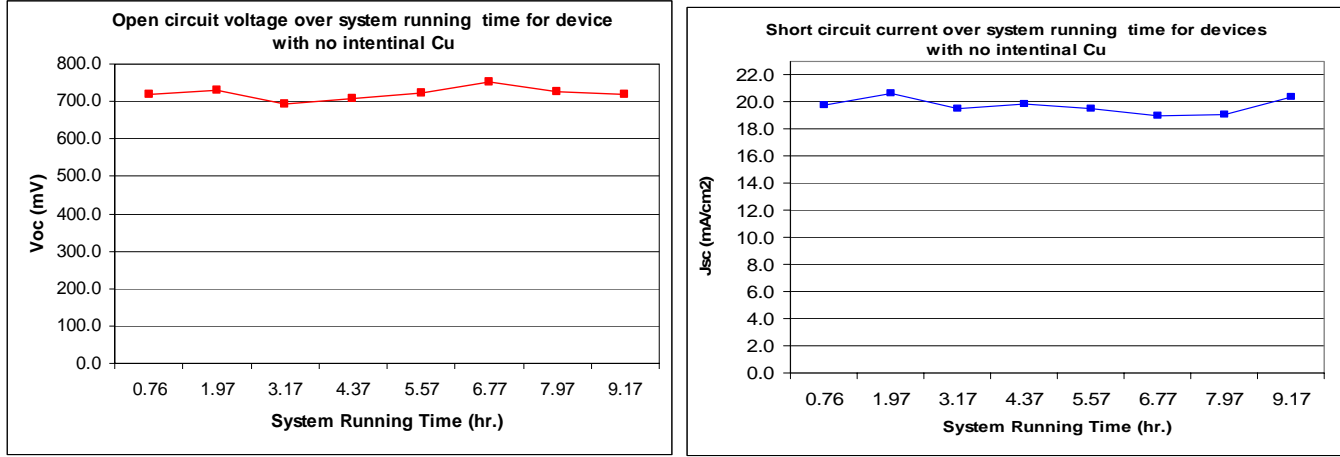
Accelerated stress testing and the exposure of devices to outdoor conditions are ongoing. Extremely long duration stress testing has demonstrated that the rate of efficiency loss levels out. The ultimate efficiency level that the devices degrade to is also dependant on process conditions. Ongoing collaborations with Larry Olsen of PNNL, and CU Boulder have progressed. A paper from our group was presented at the 19th European PV Solar Energy Conference.

2. Process Optimization

The development of hardware and the determination of optimum conditions for processing CdS, CdTe and CdCl₂, consistently over long duration system operation is a significant accomplishment of this project. This has led to the development of an optimum, baseline process for all PV fabrication steps up to the back contact formation.

During the past few months, this baseline process has been repeated for over 9 hours of operation. The Voc and Jsc parameters of devices with no intentional copper (fabricated up to but not including the back contact processing) have remained consistent for over this 9 hour time (Figures 1 and 2). This is a significant result because the CdCl₂ process conditions are a dominant factor in determining device performance and stability. As previously reported ("Progress Towards Consistent Stability", National CdTe Team Meeting, Golden, CO, July 10-11 2003), the Voc and Jsc of devices with no intentional copper can be used to predict the stability of fully processed devices. Using this metric, this repeatable, baseline process condition should result in devices with good long term stability.

During Phase II of this project, many process modules within our system were upgraded for robustness, repeatability and long term operation. These modules have been performing extremely well. The CdS, CdTe and CdCl₂ vapor sources have continued to operate very consistently for over 9 hours without replenishment or alteration of the source charge. Additional capability may be available for further



Figures 1 and 2: Open circuit voltage (Voc) and short circuit current density (Jsc) for devices processed over long duration of system operation on same source charge of CdS, CdTe and CdCl₂. Each data point is the average of either 4 or 5 devices, no data omitted.

long term operation. These process modules have proven to be quite repeatable and easy to control. The target thickness for the CdS/CdTe combined was 1.9 to 1.95 microns. For 8 processing runs (each run is over an hour long) the thickness has been maintained between 0.125 micron below and 0.5 micron above the target. The CdTe vapor source temperature was varied only 1 degree C during this time. The CdCl₂ process consistency is demonstrated in Figures 1 and 2. In addition, the chloride deposition thickness (measured by amount of substrate area where resublimation has completely occurred) has been quite repeatable. This repeatability is extremely valuable for CdTe PV process development.

The back contact copper processing is currently being optimized to achieve the same level of consistency, repeatability and long duration running capability as the other processes. The very small amount of copper used in our devices combined with the continuous nature of our system makes direct measurement of the copper deposition very challenging. As a result, controlling the copper back contact processing requires device analysis, and that the preceding processing steps remain repeatable. Additional effort, including SIMS studies, may be required. During the last quarter, over 150 separate devices have been fabricated and tested. Initial results show that for this baseline chloride process, lower substrate temperatures during copper back contact processing improves stability in 65 deg. C accelerated stress. Reduced water vapor partial pressure during device fabrication improves the devices. This optimization is ongoing.

3. Very Long Term Stability Testing

Some of our devices have been undergoing accelerated stress (lightsoaking) for almost 3.5 years. The stress conditions are 65° C, ~ 1000 W/m² illumination (cycled 5 hr. on/ 3 hr. off), open circuit bias, with a desiccated ambient. Last quarter we reported that the efficiency loss follows an exponential decay described by the function:

$$\eta = \alpha \cdot \exp\left(\frac{-t}{\lambda}\right) + \eta_{\text{sat}} \quad [1]$$

More details of this behavior are provided. For the first ~10,000 hours of lightsoaking the efficiency loss over time is relatively rapid. At approximately 20~25,000 total hours, the efficiency loss levels. The average efficiency vs. stress time data is shown in Figure 3 along with the calculated exponential decay curve fits. The curve fits are statistical and no degradation mechanism is assumed. The curve fit correlation parameters ranged from R = 0.86 ~ 0.99 for the fits shown. Calculated constants for exponential decay function [1] are listed in Table I.

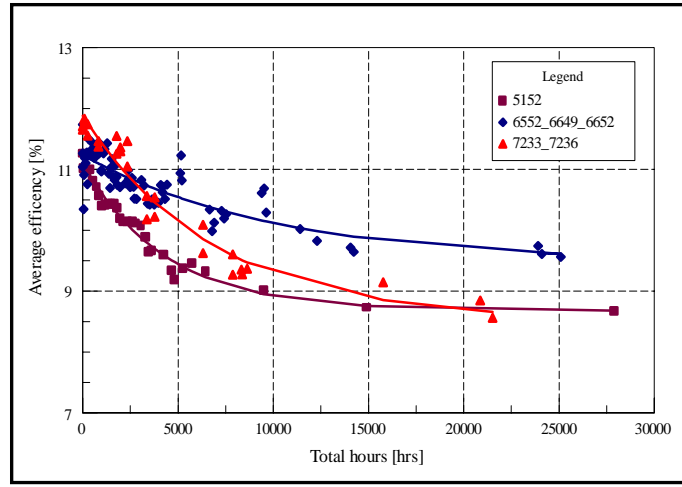


Figure 3: Long term stability plot. Each curve represents an average of at least six devices (total of 45). The data was smoothed using a Savatzky-Golay 4th order polynomial routine.

Substrate	α	λ	η_{sat} [%]	$\Delta\eta$ [% of initial]
5152	2.43	4329	8.7 ± 0.17	-21.9
6552,6652,6649	1.78	10140	9.5 ± 0.57	-14.3
7233, 7236	3.37	6853	8.5 ± 0.44	-28.3

Table I: Calculated constants for exponential decay

The very long term performance depends on processing conditions¹. The different curves in Figure 3 result from three different CdCl_2 process conditions. JV parameters for selected devices shown in Figure 3 are given in Table II. As can be seen, the main changes in JV parameters are an increase in R_{oc} and a decrease in fill factor. There is also a slight decrease in J_{sc} but essentially no change in V_{oc} . Analysis of dV/dJ vs. $1/J+JL$ curves (not shown) presents no evidence of curvature and no indication of the formation of a blocking contact.

Cell	V_{oc} [volts]	J_{sc} [mA/cm^2]	ff [%]	eff [%]	R_{oc} [ohm cm]	Stress hours [total hours]
6649-7B	768	20.33	73	11.34	0.87	0
6649-7B	763	19.80	63	9.53	2.76	23908
7233-2	729	22.67	69	11.33	0.42	0
7233-2	726	20.44	56	8.37	2.80	20866

Table II: JV parameters of selected devices from Figure 3 before and after stress of 65° C, one sun illumination (5 hr. on/ 3 hr. off), open circuit

Maintaining devices at open circuit during stress (the condition of the devices in Figure 3) is generally considered to be the most severe condition; it is expected that devices in field conditions will have superior performance. The stability of devices in outdoor conditions continues to be monitored. However, the degradation outdoors after over 2.5 years is not significant enough to develop a statistically valid correlation between the accelerated stress and outdoor conditions (if any).

4. Large Area Processing

Our group has continued with our DOE sponsored activities to develop large area processing technologies. During the last quarter additional hardware has been installed in the 16x16 inch substrate system. This will allow further thermal uniformity testing and large area deposition studies. The finite element thermal computer modeling of the large area process heads has continued in collaboration with CU

¹ R. A. Enzenroth., Barth, K. L and W. S. Sampath, "Continuous In-Line Processing of CdS/CdTe Devices: Progress Towards Consistent Stability", Presented at the 9th European PV Solar Energy Conference, 7-11, June 2004 Paris, France.

Boulder with excellent results. These are full 3D models which includes the actual geometry of the process heads, heat lamps and radiation shielding. The results from the simulation closely match experimental results. Thus the model can be useful for developing advanced process head designs. A paper on these heat transfer modeling results entitled, "Control Of Temperature Uniformity During The Manufacture of Stable Thin-Film Photovoltaic Device", has been accepted by the ASME International Mechanical Engineering Congress.

We continue to work with National Starch (the US subsidiary of ICI) to develop a strategic partnership. Proposals to obtain additional resources for the completion of the large system have been submitted. These proposals are supported by National Starch. In a recent letter, Dr. D. Miles, Global Technical Director of National Starch, states that, "Completion of this (16x16 inch substrate) system and successful trials should enable Acheson and National Starch & Chemical to develop a large-scale business based on your manufacturing technology."

5. Collaborative Activities/Additional Efforts

A. Collaborative research between our group and Larry Olsen, of Pacific Northwest National Laboratory (PNNL) has progressed. Eight CdS/CdTe devices with a special geometry were provided for his group to further investigate applying barrier coatings over our completed devices. These devices will be subjected to stress and the results reported.

B. Our collaborative work with Prof. Roop Mahajan of University of Colorado, Boulder has continued. In addition to the heat transfer modeling described above, a project is underway to develop very low cost LED lighting systems powered by PV. Initial designs have been tested with excellent results. The lighting and thermal modeling efforts are sponsored by the UN.

C. We continue to collaborate with CSM which has performed PL and EL on some of our devices. The results are being analyzed. An extensive review of the literature on thermal admittance spectroscopy has been completed.

D. Dr. Romero of NREL has performed CL analysis on some of our devices. The results of this analysis show that there is a significant increase in the CL intensity after back contact processing with copper. There is little change in the CL intensity with stress (at 65 C hours of illumination out of an 8 hour cycle open circuit conditions for approximately 3400 hrs.).

E. Measurements of the residual stress in the glass substrates after processing through our continuous system have been completed as per ASTM C1279. Glass substrates with different levels of residual stress have been sent to the ASU Photovoltaic Testing Lab for hail impact tests. These studies will establish the stress levels needed to pass the hail impact test for modules as per IEEE 1262.

F. A talk entitled "CdTe PV Technology: Low Cost Fabrication, Performance and Potential" was presented at ICS in Trieste, Italy. ICS is part of the UN.

G. A paper entitled, "Continuous, In-Line Processing Of CdS/CdTe Devices: Progress Towards Consistent Stability," was presented at the 19th European PV Solar Energy Conference in Paris, France. A copy is enclosed.

If you have any questions, please do not hesitate to call the laboratory at 970.491.8411. Thank you.

Sincerely,

W. S. Sampath
Associate Professor
Colorado State University

C: Carolyn Lopez

Enclosure